ABSTRACT OF THE INVENTION

A system and method is described for a driver circuit used for high speed data transmission in LVDS and CML transceiver device applications. The transceivers are intended to receive a low voltage differential input signal and interchangeably drive a standard LVDS load with a TIA/EIA-644 compliant LVDS signal, and a standard CML load with a standard CML compatible signal. The driver circuit operates at speeds up to 1.36Gbps, making it compatible with the OC-24 signaling rate for optical transmission. To accomplish this, the driver uses a mixed combination of voltage and current mode drive sections in the output circuit when coupled to LVDS loads, and when the driver is coupled to CML loads, operates purely in a current mode using only the current mode drive section. MOS transistors and a current source are used in the current mode switch portion to switch the drive with a constant current at the high speeds, and NPN transistors in the voltage mode output portion provide variable impedance for the output circuit. A common mode compensation circuit using a feedback voltage from the load generates a compensation signal for variable impedance control of the NPN transistors to yield a regulated voltage for the common mode dc voltage.